Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-11. (Cancelled)

12. (Currently Amended) A protective circuit comprising:

a first transceiver to connect to a first network section;

a second transceiver to connect to a second network section; and

a logic isolation circuit to isolate a network section from a bus system network using logic when a fault state is recognized in the network section, the logic isolation circuit comprising

a reception ~~multiplexers~~ multiplexer having a first signal input connected to the first transceiver receiver and a second signal input to receive a logically recessive transmission signal; and

a transmission ~~multiplexers~~ multiplexer having a signal output connected to one of the transceiver transmitters and a first signal input connected to a signal output of the reception ~~multiplexers~~ multiplexer for the transceiver receiver, wherein a logically recessive transmission signal is applied to the second signal input of the ~~multiplexers~~ multiplexer;

~~a first transceiver to connect to a first network section;~~

~~a second transceiver to connect to a second network section; and~~

wherein a first transceiver receiver in the first transceiver recognizes a fault state in the first network section, and a second transceiver receiver in the second transceiver recognizes a fault state in the second network section, and the logic isolation circuit includes logic signal inputs to connect to both receivers and logic signal outputs to connect to transceiver transmitters.

13. (Canceled)

14. (Previously Presented) The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal from the first network section.

15. (Previously Presented) The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal to the second network section.

16. (Previously Presented) The protective circuit of claim 12 further comprising a fault bus to connect the logic isolation circuit to control nodes in the bus system network, wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

17. (Currently Amended) The protective circuit of claim [[13]] 12 wherein the first signal inputs of the transmission multiplexers [[is]] are connected to the signal outputs of the reception multiplexers with DC decoupling.

18. (Currently Amended) A protective circuit for an access arbitrated bus system network, the protective circuit comprising:

a fault recognition device to recognize a fault state in a network section in the bus system network by monitoring voltage levels on a plurality of bus lines in the bus system network; and

a switching device to isolate the network section from the bus system network by switching bus lines when a fault state has been recognized in the network section, the switching device including a first switch and a second switch ~~plurality of switches~~ connected in parallel, wherein the first switch is associated with a first bus line of the plurality of bus lines and the second switch is associated with a second bus line of the plurality of bus lines. ~~the switches comprising two reverse-connected series MOSFET transistors~~.

19. (Previously Presented) The protective circuit of claim 18 wherein the fault recognition device comprises:

a first fault state detection circuit to detect a fault state in a first network section;

a second fault state detection circuit to detect a fault state in a second network section; and

a fault recognition logic circuit connected to the first and the second fault state detection circuits which outputs a control signal to the switching device to isolate the first and the second network sections when the first or the second fault state detection circuits detect a fault state.

20. (Currently Amended) The protective circuit of claim 19 further comprising a fault bus to connect [[the]] the fault recognition logic circuit to control nodes in the bus system network wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

21. (Previously Presented) The protective circuit of claim 18 wherein the access arbitrated bus system is a Controller Area Network (CAN) bus system.

22. (Previously Presented) The protective circuit of claim 18 wherein the access arbitrated bus system is a J 1850 bus system.

23. (Previously Presented) The protective circuit of claim 18 wherein the access arbitrated bus system is a Carrier Sense Multiple Access (CSMA) bus system.

24. (Previously Presented) The protective circuit of claim 18 wherein the fault recognition device recognizes as fault states, short circuits between the bus lines in a network section, short circuits between the bus lines in the network section and ground, and short circuits between the bus lines in the network section and supply voltage.

25. (Currently Amended) The protective circuit of claim 18 wherein the fault recognition device recognizes the termination of a fault state in a network section and actuates the ~~isolation device~~ switching device to remove the isolation between the network sections and the overall bus system.

26. (New) A protective circuit for an access arbitrated bus system network, the protective circuit comprising:

a fault recognition device to recognize a fault state in a network section in the bus system network by monitoring voltage levels on bus lines in the bus system network; and

a switching device to isolate the network section from the bus system network by switching bus lines when a fault state has been recognized in the network section, the switching device including a plurality of switches connected in parallel, wherein a respective switch is provided for each bus line, wherein the switches comprise semiconductor switches configured to block signals in both signal directions.